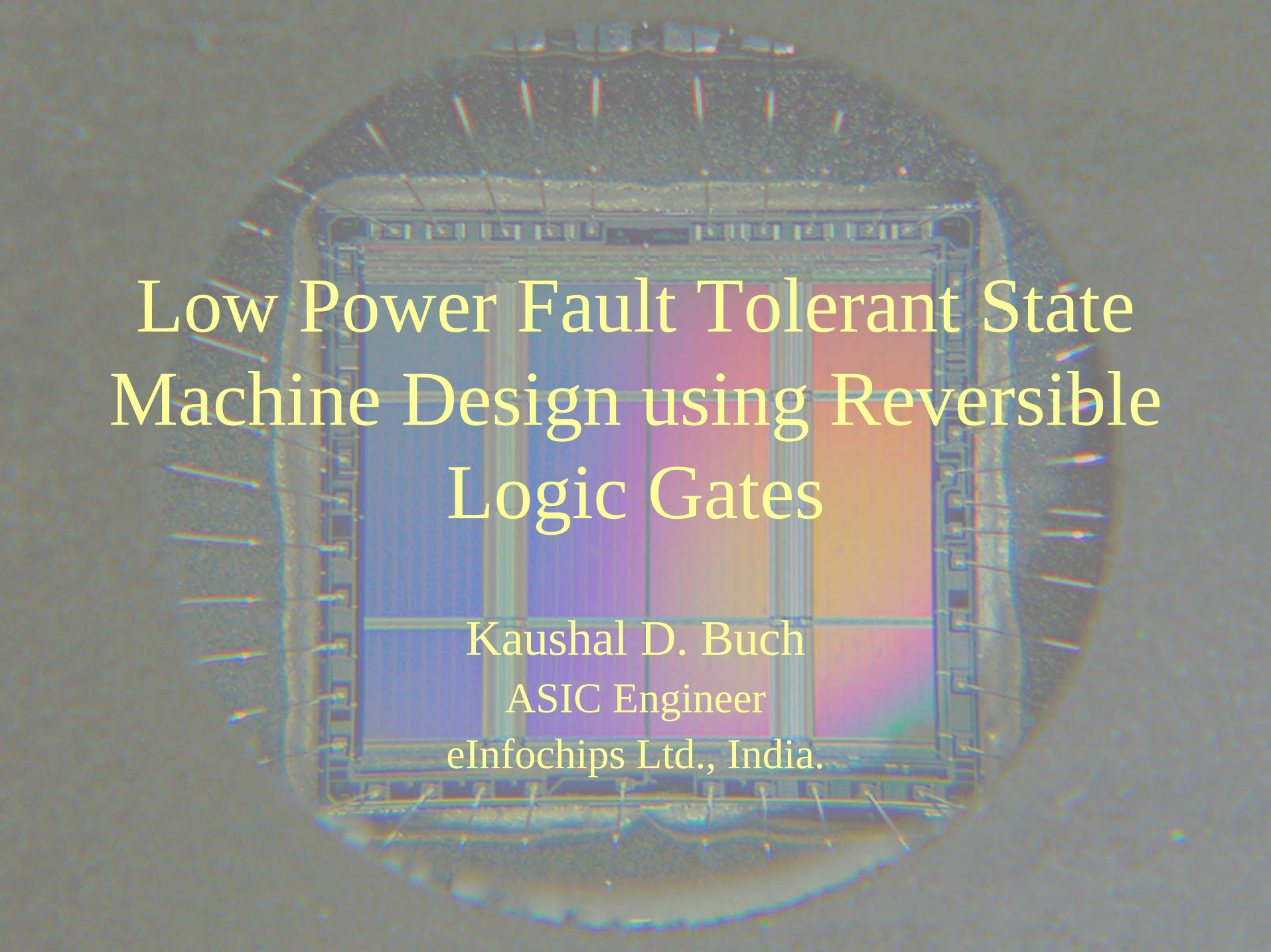

Low Power Fault Tolerant State Machine Design using Reversible Logic Gates

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Abstract

A novel approach for developing a fault-tolerant state machine using reversible logic gates is proposed. The uniqueness of this approach lies in the fact that the design of such state machines using reversible gates is largely unexplored and harnesses promising results. Reversible logic gates are known to have power dissipation less than KTln2 joules for each logic bit computation and as a consequence low power fault tolerant state machines designed using them may prove to be quite useful during operation of circuits in random noise environments, which might lead to single event upsets (SEU). The designs of combinational and sequential logic circuits needed for the development of fault-tolerant state machine were done primarily using Fredkin and Feynman reversible logic gates. Their major advantage over the conventional fault tolerant state machine would be very low power consumption. The Hamming-3 and Hamming-2 type of state machine encoding for fault tolerant design were considered and the error detection and correction circuits were also designed using reversible gates

Reversible Logic

- It is found that each logic operation consumes KTln2 joules per bit[1,2].
- Logic reversibility helps reducing the power dissipating in the form of heat [1].
- Several logic gates have been proposed theoretically considering the limitations posed by the theory of logic reversibility.

Properties of reversible logic gates

1. Minimum input constants
2. Minimum number of gates
3. Minimum number of garbage outputs

Garbage outputs are those outputs which are not used further for any computation.

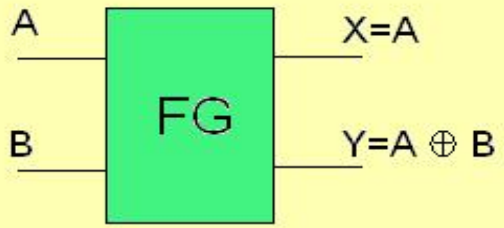
Characteristics of reversible logic circuits

- There has to be one to one correspondence between inputs and outputs.
- Feedback and Fanout are not allowed.

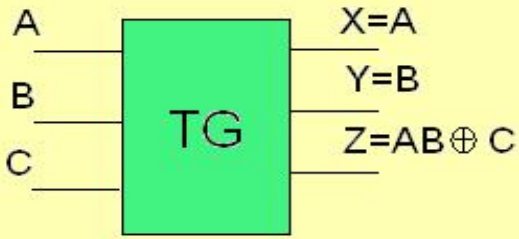
Solutions –

- Gates that have one to one correspondence can only be used at each stage in the circuit e.g. Fredkin, Toffoli, Feynman , Peres gate etc.
- Fanout and feedback can be achieved using copying gate – Feynman and Double Feynman gates

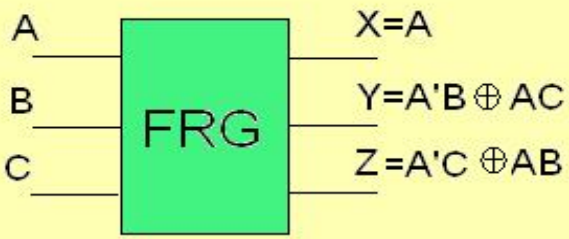
Various Types of Reversible Logic Gates



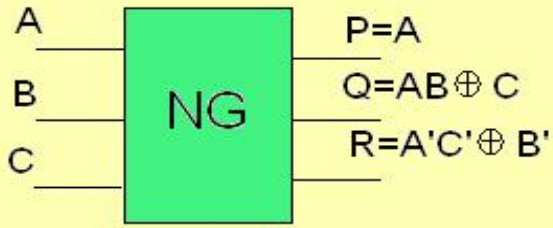
Feynman Gate



Toffoli Gate

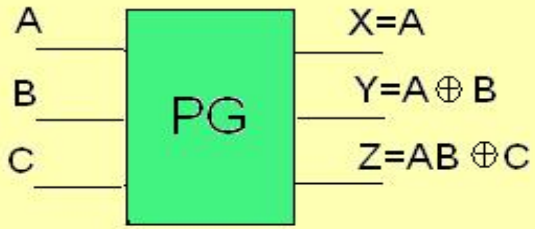


Fredkin Gate



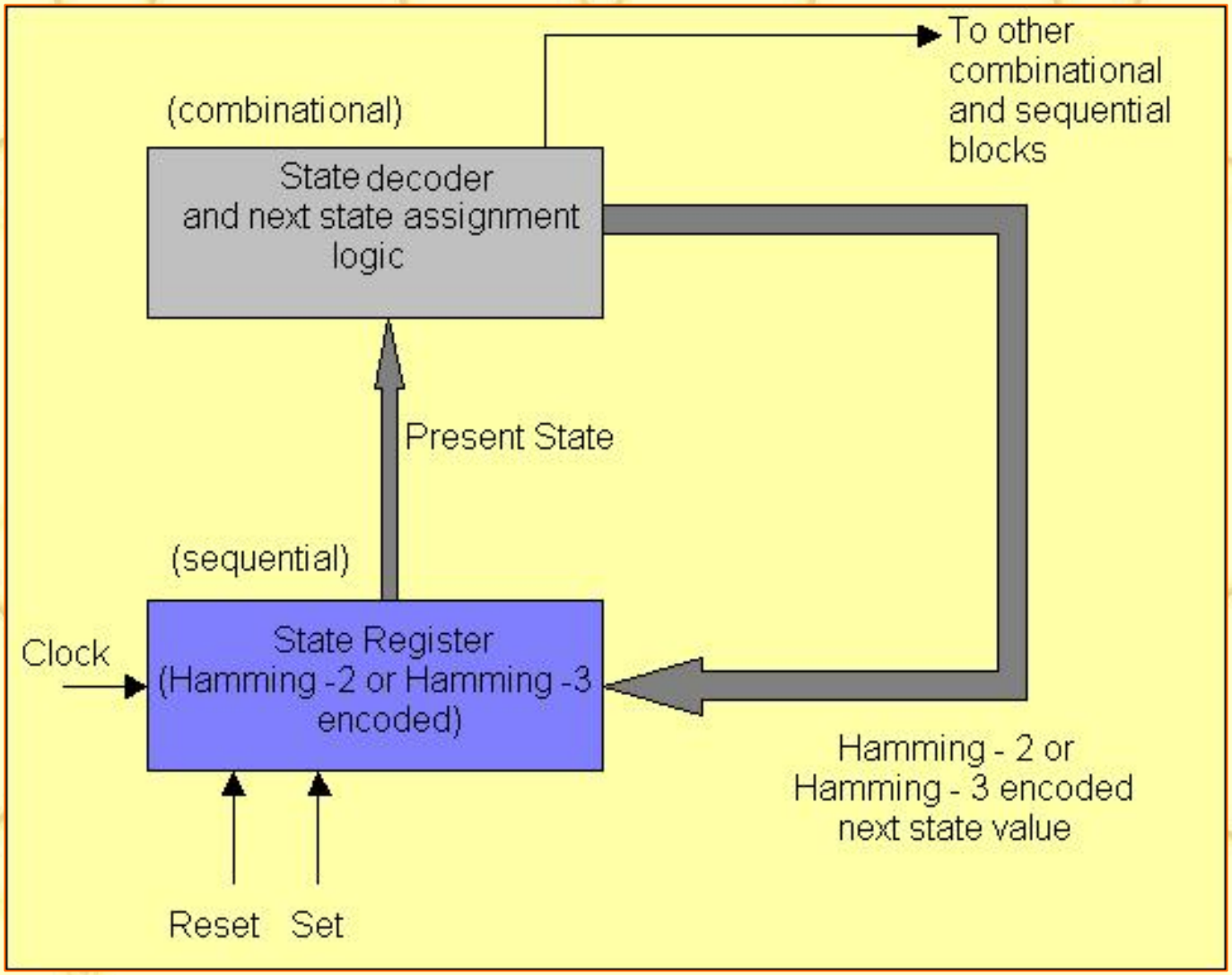
New Gate

Double Feynman Gate

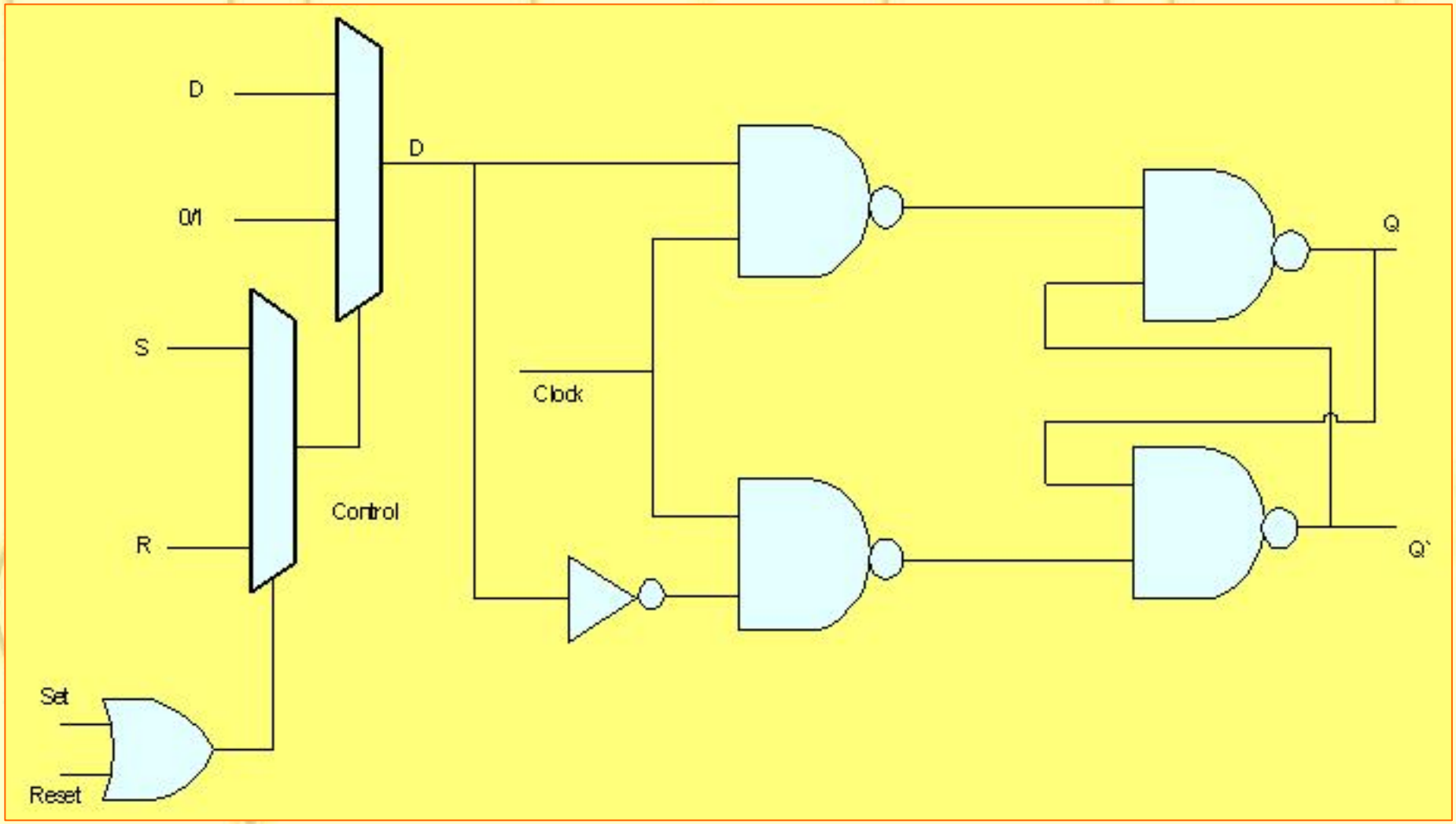


Peres Gate

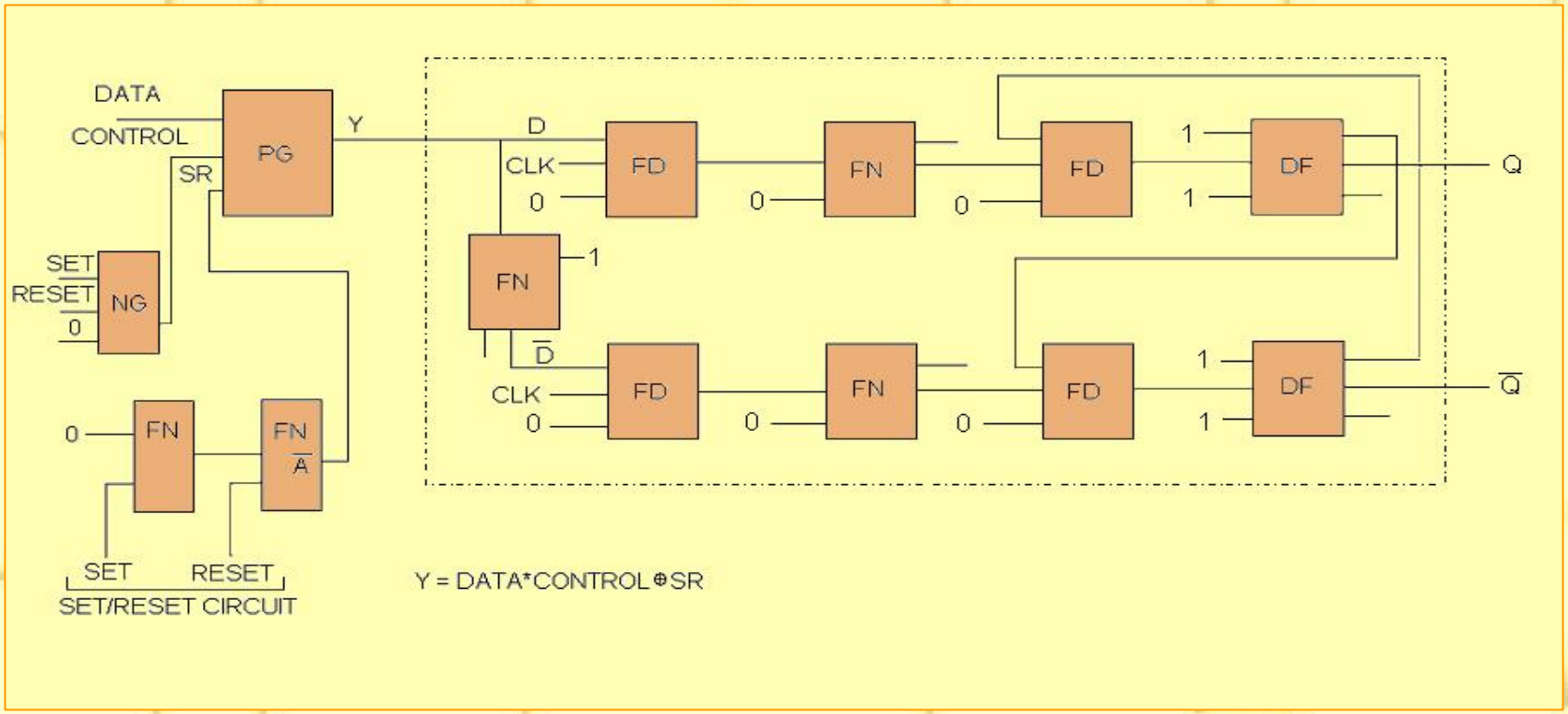
Basic Fault Tolerant State Machine



Logic Circuit for D Flip-Flop



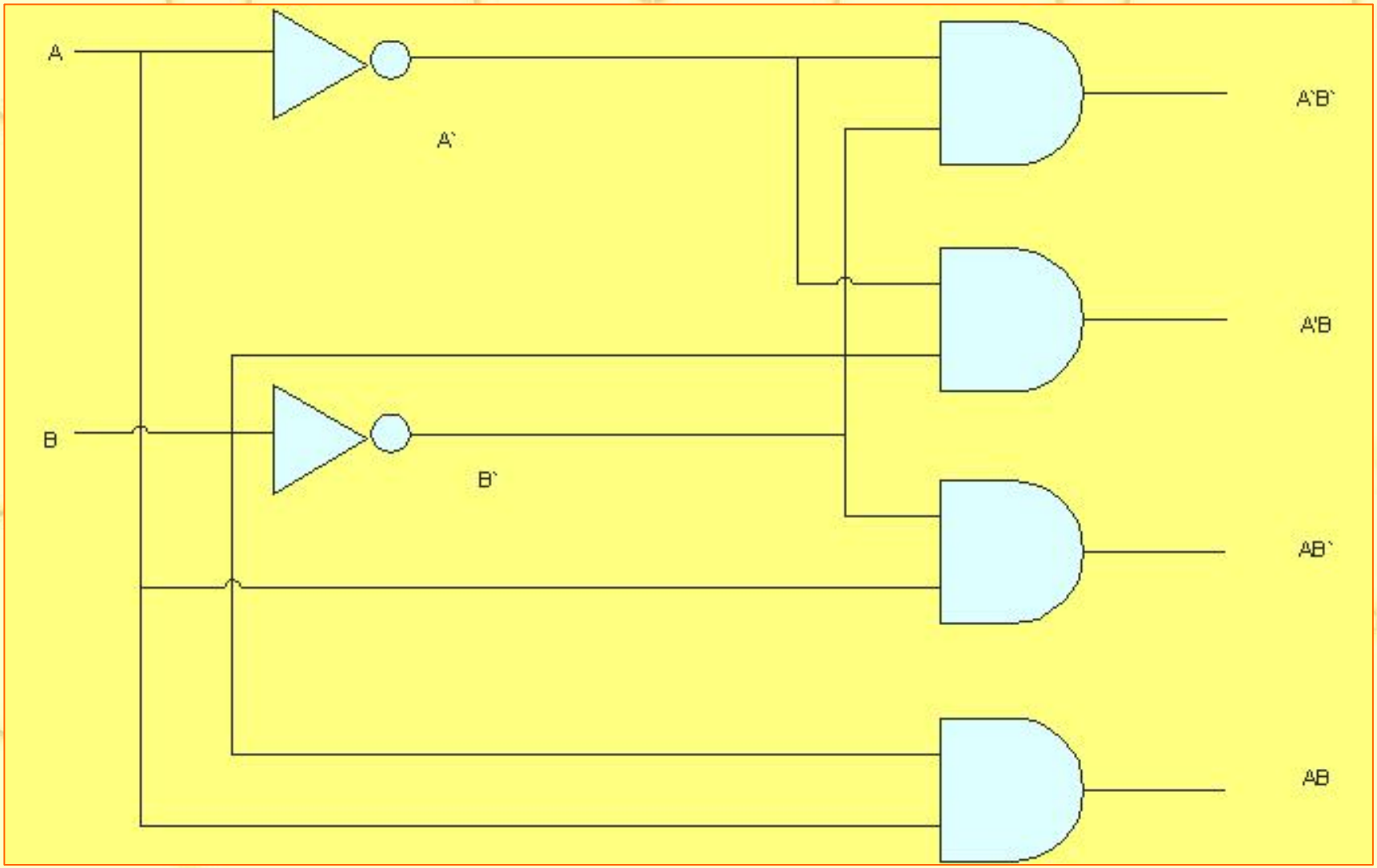
D-Flip Flop using reversible logic gates



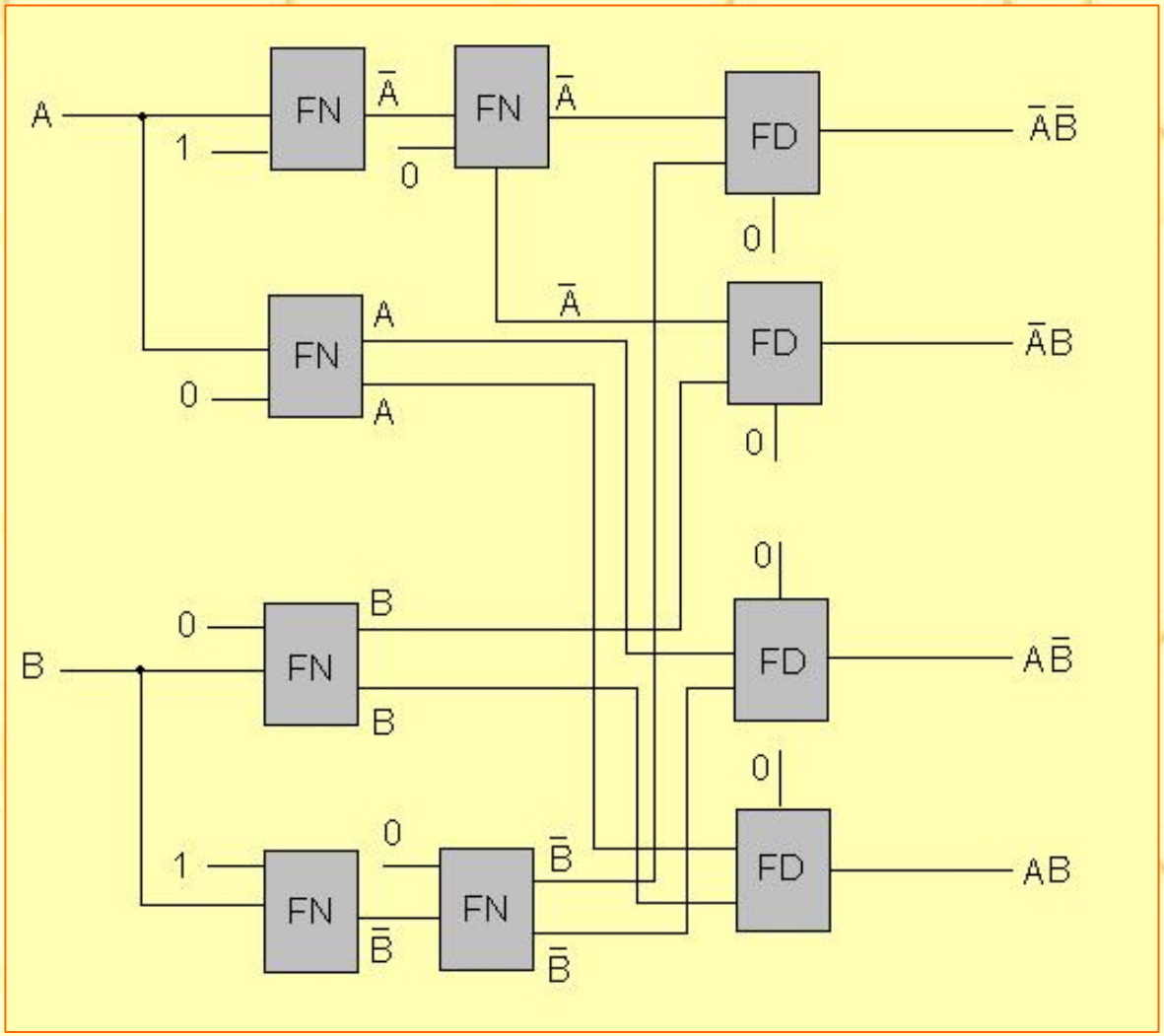
FD: Fredkin Gate FN: Feynman Gate DF: Feynman Double Gate PG: Peres Gate

- The DFF shown above is an extension of that shown in [3]. It has additional asynchronous set/reset logic, which is necessary when using it as a register in a state machine.

Logic Circuit for 2 x 4 Decoder



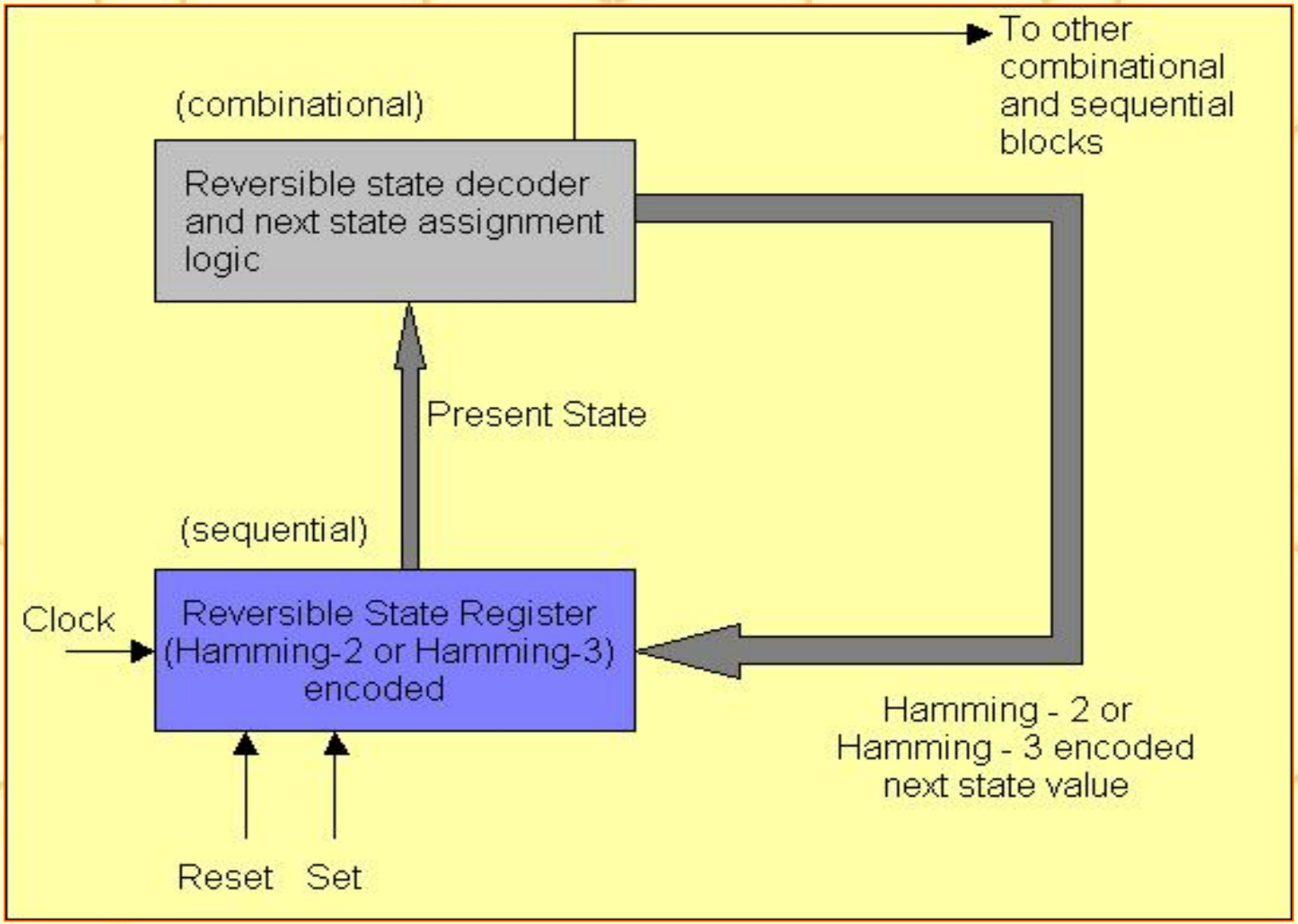
Decoder using Reversible gates



State Machine

- Using the reversible D-Flip Flops as register for storing the current state and decoder to compute and update the state register to next state value, a state machine has been developed. The entire figure is not given as it becomes quite difficult to fit in the space.
- The state update can be binary, one-hot or Hamming 2 or 3 encoded. The state machine currently under review is made considering the Hamming 2 or 3 state encoding as it is to be made fault tolerant.

Fault Tolerant State Machine using Reversible gates



Conclusion

- The design of state machine using reversible logic gates, which has been described here, has a reversibility in logic at every interface between the logic gates and across the circuits. At any point in the whole circuit, it is possible to map and trace back the output to a unique input, which satisfies the criteria for reversible systems.
- A fault tolerant state machine using reversible gates was presented. It was an extension of existing work which was restricted to only basic digital circuit design using reversible logic gates.
- This previously unpublished concept unravels a possibility to implement such very low power state machines. Such designs would be extremely useful for space applications, where power consumption is of primary concern.
- Also novel approaches to design of reversible D-FF and decoders were shown.
- The concept seems to be quite promising for quantum computing.

References

1. R. Landauer, “Irreversibility and Heat Generation in the Computing Process”, IBM Journal, July 1961.
2. Bennett, C.H., “Logical Reversibility of Computation”, IBM Journal of Research and Development, November 1973.
3. H. Thapliyal, Srinivas M.B. and M. Zwolinski, “A Beginning in the Reversible Logic Synthesis of Sequential Circuits”, MAPLD 2005.